Implementation of all digital phase locked loop

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Received: April 29, 2018 Accepted: May 30, 2018

ABSTRACT *The paper presents an all-digital phase locked loop (PLL). PLL is a closed-loop control system that is used for the purpose of synchronization of phase and frequency with that of an incoming signal. The most versatile application of PLL is for clock generation and clock recovery in microprocessor and communication systems. Nowadays, due to higher integration of digital designs, digital PLL are preferred. The present work focuses on the design of ADPLL using tool from Xilinx. Code for ADPLL is written in Verilog and compiled using NCVerilog.*

Index Terms— *All digital PLL, Soc Encounter, NCVerilog.*

INTRODUCTION

The steady improvement of components for digital applications, more applications pertaining to processing signals are experiencing a shift from the analog to the digital domain. The digital domain compared to the analog domain provide manifold benefits like easy calibration, higher accuracy, better predictability and the probability to increase the complexity without the need for tedious adjustments or calibrations. Thus the digital domain certainly provides a better edge over analog domain which attracts more research and experimentation in this field of study.

A. History of PLL

Automatic synchronization of electronic oscillators was described in 1923 [1]. Earliest research towards what became known as the phase-locked loop goes back to 1932, when British researchers developed an alternative to Edwin Armstrong's superheterodyne receiver, the Homodyne or direct-conversion receiver. In the homodyne or synchrodyne system, a local oscillator was tuned to the desired input frequency and multiplied with the input signal. The resulting output signal included the original modulation information. The intent was to develop an alternative receiver circuit that required fewer tuned circuits than the superheterodyne receiver. Since the local oscillator would rapidly drift in frequency, an automatic correction signal was applied to the oscillator, maintaining it in the same phase and frequency as the desired signal. The technique was described in 1932, in a paper by Henri de Bellescize, in the French journal L'OndeÉlectrique [2].

When Signetics introduced a line of monolithic integrated circuits such as the NE565 that were complete phase-locked loop systems on a chip in 1969, applications for the technique multiplied [3]. A few years later RCA introduced the "CD4046" CMOS Micropower Phase-Locked Loop, which became a popular integrated circuit.

Since its inspection in early 1930s, where it was used in the synchronization of the horizontal and vertical scans of television, it has come to an advanced form of integrated circuit (IC). Today found uses in many other applications. The first PLL ICs were available around 1965; it was built using purely analog component. Recent advances in integrated circuit design techniques have led to the development of high performance PLL which has become more economical and reliable. Now a whole PLL circuit can be integrated as a part of a larger circuit on a single chip.

B. Motivation

Nature is analog and so are the circuits that drive wireless communication. But analog devices are generally harder to miniaturize and have slowly been ceding ground to digital components. Radio-frequency circuits are especially sensitive to design changes, and the properties of analog components like inductors don’t improve as the devices get smaller. As a result, analog chips tend to lag behind their all-digital counterparts by a couple of manufacturing-process generations, which means that their features are much less fine.

Over the years, Digital circuits have taken over a bit more of the analog domain. And the poster child of this trend is Phase locked loop (PLL), a core communication block which is implemented using digital circuits. The main advantage of all digital implementation is that the circuits get faster and occupy lesser area with a newer manufacturing process.

Phase locked loop (PLL) is the heart of the many modern electronics as well as communication system. Recently plenty of the researches have conducted on the design of phase locked loop (PLL) circuit and still research is going on this topic. Most of the researches have conducted to realize a higher lock range PLL with lesser lock time and have tolerable phase noise. The most versatile application of the phase locked loops (PLL) is for clock generation and clock recovery in microprocessor, networking, communication systems, and frequency synthesizers. Phase locked-loops (PLLs) are commonly used to generate well-timed on-chip clocks in high-performance digital systems.

C. **Literature Survey**

Ronald E Best [4] gives an introduction to PLL and deals with theory, design and applications of Mixed PLLs and Digital PLLs. The discussion includes different types of phase detector (linear and digital), phase frequency detectors with charge pump, Loop Filter and VCOs/NCOs.

Shabaany [5], presents a 0.7-to-1.1-GHz all-digital phase locked loop with a new phase frequency detector and controlled oscillator with body-biasing is presented. Digital-to-voltage converter is controlled the bulk voltage in proposed voltage controlled oscillator, which results high frequency resolution and low power consumption. A search algorithm was used to generates the digital code for the digital-to-voltage converter. This all-digital phase locked loop uses a new structure for the phase-frequency-detector, which ensures high accuracy at phase frequency detecting and increasing lock speed. The proposed design was evaluated in PTM 65nm. The power consumption of the proposed circuit at 900 MHz frequency is 4.8mW.

Kumm, M [6] presents an all-digital phase-locked loop (ADPLL), and it is implemented on a field-programmable gate array. All components like the phase detector (PD), oscillator, and loop filter are realized as digital discrete-time components fed from analog-to-digital converters. The phase detection is realized by generating first an analytic signal using a compact implementation of the Hilbert transform and then computing the instantaneous phase with the CORDIC algorithm. A phase-unwrap component was realized, which extends the linear range of the PD, so that the linear model is valid in the full frequency range. This property leads to a constant lock-in time for arbitrary frequency changes. An analytic solution for the lock-in frequency range and the stability range including processing delays is given. All relations to design an ADPLL of the presented structure are derived. A detailed example application of an ADPLL designed as an offset local oscillator was given.

Das A.[7] presents a linear all-digital phase locked loop based on FPGA. In this ADPLL the phase detection system is realized by generating an analytic signal using a compact implementation of Hilbert transform and then simply computing the instantaneous phase using CORDIC algorithm in vectoring mode of operation. A 16-bit pipelined CORDIC algorithm is employed in order to obtain the phase information of the signal. All the components used in this phase detection system are realized as digital discrete time components. This design did not involve any class of multipliers thus reducing the complexity of the design. The loop filter of the ADPLL has been designed using PI controller which has a low pass behavior and is used to discard the higher order harmonics of the error signal. The CORDIC algorithm in its rotation mode of operation was used to compute sinusoidal values for the DDS. The ADPLL model was implemented using Xilinx ISE 12.3 and ModelSim PE Student Edition 10.1a.

Our work is based on Sharma[8]. In this work, a design of an All-Digital Phase Locked Loop (ADPLL) IP core using an accumulator type DCO is proposed in order to generate desired frequency signals. Faster and efficient operation of PLLs was very much desired. Implementation of a digital PLL on a FPGA was used to control the jitter involved in the operation of PLLs to a greater extent that is troubling the current communication industry.

PHASE LOCKED LOOP

A phase-locked loop or phase lock loop (PLL) is a control system that generates an output signal whose phase is related to the phase of an input signal. While there are several differing types, it is easy to initially visualize as an electronic circuit consisting of a variable frequency oscillator and a phase detector. The oscillator generates a periodic signal. The phase detector compares the phase of that signal with the phase of the input periodic signal and adjusts the oscillator to keep the phases matched. Bringing the output signal back toward the input signal for comparison is called a feedback loop since the output is 'fed back' toward the input forming a loop [9].

Keeping the input and output phase in lock step also implies keeping the input and output frequencies the same. Consequently, in addition to synchronizing signals, a phase-locked loop can track an input frequency, or it can generate a frequency that is a multiple of the input frequency. These properties are used for computer clock synchronization, demodulation, and frequency synthesis, respectively.

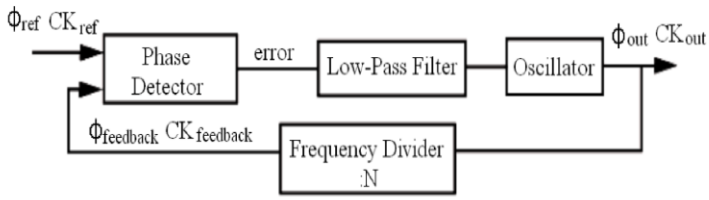
Phase-locked loops are widely employed in radio, telecommunications, computers and other electronic applications. They can be used to demodulate a signal, recover a signal from a noisy communication channel, generate a stable frequency at multiples of an input frequency (frequency synthesis), or distribute precisely timed clock pulses in digital logic circuits such as microprocessors. Since a single integrated circuit can provide a complete phase-locked-loop building block, the technique is widely used in modern electronic devices, with output frequencies from a fraction of a hertz up to many Gigahertz [9].

Some of the applications of PLL are Clock Recovery, De-Skewing, Clock Generation, Spread Spectrum, Clock Distribution, Jitter and noise reduction, Frequency Synthesis [10-13].

D. **Structure of PLL**

Phase-locked loop mechanisms may be implemented as either analog or digital circuits. Both implementations use the same basic structure. Both analog and digital PLL circuits include four basic elements [4]:

- Phase detector,
- Low-pass filter,
- Variable-frequency oscillator, and
- Feedback path which may include a frequency divider.



E. **Phase Detector**

The two inputs of the phase detector are the reference input and the feedback from the VCO. The PD output controls the VCO such that the phase difference between the two inputs is held constant, making it a negative feedback system. There are several types of phase detectors in the two main categories of analog and digital. Different types of phase detectors have different performance characteristics [4].

For instance, the frequency mixer produces harmonics that adds complexity in applications where spectral purity of the VCO signal is important. The resulting unwanted (spurious) sidebands, also called "reference spurs" can dominate the filter requirements and reduce the capture range and lock time well below the requirements. In these applications the more complex digital phase detectors are used which do not have as severe a reference spur component on their output. Also, when in lock, the steady-state phase difference at the inputs using this type of phase detector is near 90 degrees. The actual difference is determined by the DC loop gain.

A bang-bang charge pump phase detector must always have a dead band where the phases of inputs are close enough that the detector detects no phase error. For this reason, bang-bang phase detectors are associated with significant minimum peak-to-peak jitter, because of drift within the dead band.[citation needed] However these types, having outputs consisting of very narrow pulses at lock, are very useful for applications requiring very low VCO spurious outputs. The narrow pulses contain very little energy and are easy to filter out of the VCO control voltage. This results in low VCO control line ripple and therefore low FM sidebands on the VCO.

In PLL applications it is frequently required to know when the loop is out of lock. The more complex digital phase-frequency detectors usually have an output that allows a reliable indication of an out of lock condition.

F. **Loop Filter**

The block commonly called the PLL loop filter, usually a low pass filter generally has two distinct functions [4].

The primary function is to determine loop dynamics, also called stability. This is how the loop responds to disturbances, such as changes in the reference frequency, changes of the feedback divider, or at startup. Common considerations are the range over which the loop can achieve lock (pull-in range, lock range or capture range), how fast the loop achieves lock (lock time, lock-up time or settling time) and damping behavior. Depending on the application, this may require one or more of the following: a simple proportion (gain or attenuation), an integral (low pass filter) and/or derivative (high pass filter). Loop

parameters commonly examined for this are the loop's gain margin and phase margin. Common concepts in control theory including the PID controller are used to design this function.

The second common consideration is limiting the amount of reference frequency energy (ripple) appearing at the phase detector output that is then applied to the VCO control input. This frequency modulates the VCO and produces FM sidebands commonly called "reference spurs". The low pass characteristic of this block can be used to attenuate this energy, but at times a band reject "notch" may also be useful.

The design of this block can be dominated by either of these considerations, or can be a complex process juggling the interactions of the two. Typical trade-offs are: increasing the bandwidth usually degrades the stability or too much damping for better stability will reduce the speed and increase settling time. Often also the phase-noise is affected.

G. **Oscillator**

All phase-locked loops employ an oscillator element with variable frequency capability. This can be an analog VCO either driven by analog circuitry in the case of an APLL or driven digitally through the use of a digital-to-analog converter as is the case for some DPLL designs. Pure digital oscillators such as a numerically controlled oscillator are used in ADPLLs [4].

H. **Feedback Path and Divider**

PLLs may include a divider between the oscillator and the feedback input to the phase detector to produce a frequency synthesizer. A programmable divider is particularly useful in radio transmitter applications, since a large number of transmit frequencies can be produced from a single stable, accurate, but expensive, quartz crystal–controlled reference oscillator.

Some PLLs also include a divider between the reference clock and the reference input to the phase detector. If the divider in the feedback path divides by N and the reference input divider divides by M, it allows the PLL to multiply the reference frequency by N/M. It might seem simpler to just feed the PLL a lower frequency, but in some cases the reference frequency may be constrained by other issues, and then the reference divider is useful.

Frequency multiplication can also be attained by locking the VCO output to the Nth harmonic of the reference signal. Instead of a simple phase detector, the design uses a harmonic mixer (sampling mixer). The harmonic mixer turns the reference signal into an impulse train that is rich in harmonics. The VCO output is coarse tuned to be close to one of those harmonics. Consequently, the desired harmonic mixer output (representing the difference between the N harmonic and the VCO output) falls within the loop filter pass-band.

It should also be noted that the feedback is not limited to a frequency divider. This element can be other elements such as a frequency multiplier, or a mixer. The multiplier will make the VCO output a sub-multiple (rather than a multiple) of the reference frequency. A mixer can translate the VCO frequency by a fixed offset. It may also be a combination of these. An example being a divider following a mixer; this allows the divider to operate at a much lower frequency than the VCO without a loss in loop gain.

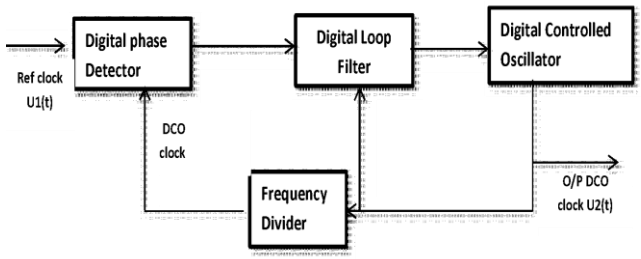
IMPLEMENTATION OF ADPLL

The all-digital PLL offers various advantages compared to other types due to the use of only digital signals. The ADPLL has three components namely [13]

- Digital Phase Detector
- Loop Filter
- Digital controlled Oscillator

The task of a PLL is to lock the phase and the frequency of U1(t) to those of U2(t). The phase detector is used to detect the difference between U1(t) and U2(t). The loop filter is used to filter out out-of-band noise. Finally, the voltage-controlled oscillator (VCO) receives the output of the loop filter and adjusts the phase/frequency of the output signal U2(t) accordingly.

To realize an ADPLL, all function blocks of the system must be implemented by purely digital circuits. The signal are digital (binary) and may be a single digital signal or a combination of parallel digital signals. There are some advantages: No off-chip components and Insensitive to technology [13].



DIGITAL PHASE DETECTOR(DPD)

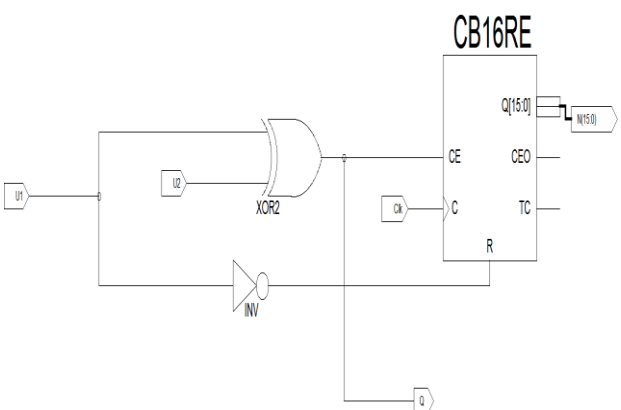
Phase Detector (PD) is used to detect the phase difference between the reference signal and the required signal. The PD was the only component that was digitized long back. It's used in the Digital PLL . Similar idea can be extended to the ADPLL.

The three common implementations of the digital PD are:

1. Exclusive-or (EXOR) Gate
2.Edge triggered JK Flip-Flop
3.Digital Phase-Frequency Detector

In this paper we are considering EX-OR gate based DFD.The EXOR mechanism offers a simple yet reliable method of phase detection. Here the reference signal $U_1(t)$ and the feedback signal $U_2(t)$ are provided to the inputs of a XOR gate.This type of detector locks itself 90 degree behind the phase of the input signal.

This XOR gate can be used in conjunction with a counter to output the phase error. For this we have implemented a N counter. The circuit diagram of this block is as shown below:



Fig(ii) Digital phase detector in Xilinx.

WORKING

Along with the XOR gate we have also included a 15 bit counter to measure the phase error. The XOR gate output Q acts as the clear signal for the counter and the reference signal U_1 acts as a reset (negative logic) for the counter. The signal U_2 is actually obtained as a feedback signal from the Digital controlled oscillator. To test the working of this model we have forced the inputs U1 and U2 in the ISE simulator. The counter counts on the positive edge of the clock. The clock frequency is given by,

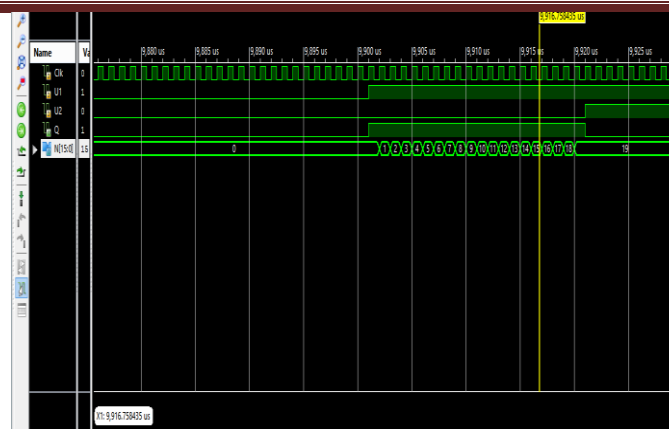
$F_{clk}=M.f_{ref}$ (1)

The parameters are as follows.

• Clock frequency: 1.6 MHz which is F_{clk}

• U_1 and U_2: Frequency of 100 KHz with a phase difference of 720 which is nothing but the reference frequency F_{ref}.

Hence The value of M in equation 1 is 16. The Xilinx Screenshot of this implementation is as shown below:



Fig(iii) Screenshot of Digital phase detector simulation using Xilinx.

In the above screen shot we can see that whenever the Q output is one and also the reference signal is high the counter starts the count. After that when Q goes to zero the count is held and for U1 the count value is reset. Though the value of N is not passed to the next block it is required in order to note down the scale of error (i.e. phase difference).

LOOP FILTER (LF)

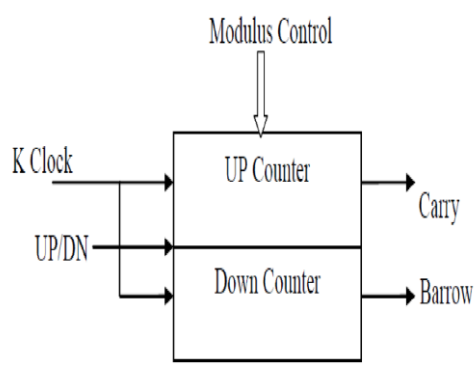
The digital loop filter is not always present in phase locked loops. But in higher order loops where applications such as servo control, telecommunications are involved the digital loop filter is necessary. Different Phase Detectors generate different types of signals. It removes high frequency parts of phase error signal

Usually two types of Loop filters are widely used namely

1. K Counter based Loop filter
2. Up/ Down counter based loop filter

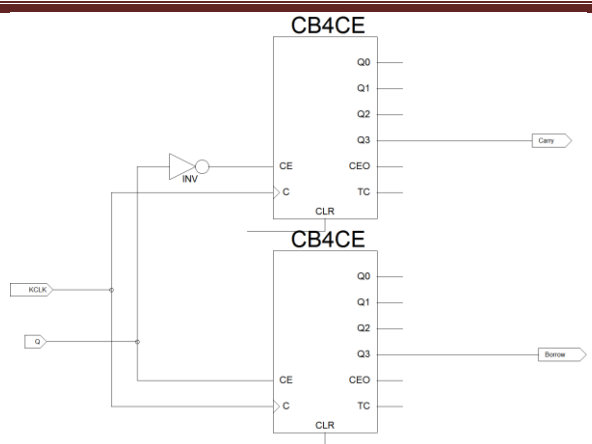
In K counter based loop filter two separate counters are used whereas in the UP/Down counter based a single counter is used preceded by a pulse forming circuit.

In this paper we have used a K counter based loop filter and its block diagram is as shown below:



Fig(v) Block diagram of K counter based loop filter.

In this counter the dn/up signal is nothing but the Q signal generated from the digital frequency detector. The circuit diagram of the counter is shown in fig (vii). Here as we can see that the UP/DN signal which is provided to "Counter enable (CE)" is 'Q' signal from the previous block. The Kclkis the high frequency clock fed to both the counters..Fig(vi) shows the Xilinx implementation of the K counter based loop filter.



Fig(vi) Xilinx implantation of K counter based loop filter

WORKING.

In our paper to maintain synchronization we have fed both the digital frequency detector and the up and down counters with the same clock.

So Kclk here and clk previously are same. Both UP and DOWN counters in our case are 4 bit counters.

In the above circuit we can also see that carry and borrow are taken from Q3 or the MSBs of the UP and DOWN counter respectively. This is because the value of a number in the range 0 to K-1 becomes greater than K/2 only if the MSB goes high. Hence we have taken the Q3 bits as carry and borrow respectively

The $K\text{-}_{clk}$ frequency is decided by the equation,

$F_{k\text{-}clk}=2*N*F_{ref.}$ (2)

We have taken the value of N to be 8 to make $F_{k\text{-}clk}$ to be same as F_{ref} as explained earlier.

So M=2*N=16.

So all the events are controlled by a single clock of frequency 1.6 MHz.

The waveform for the Loop filter are as shown in fig(viii). Here we also have included the signals from the digital frequency oscillator for the sake of clarity. The clk in the waveform is nothing but K-clk only and it is forced to frequency of 1.6 MHz. The U1 and U2 signals like earlier are each forced to 10 KHz with the former leading the latter by 720. The carry and borrow signals are obtained from the most significant bits of the up and down counters as shown.

The value of K is set to 16. Hence, the down counter counts from 0 to 15 whenever the signal Q is high. Similarly when Q is zero the up counter counts from 0 to 15. As discussed earlier whenever the count is in the range [8,15] the MSD is 1 and hence depending on the whether we are considering up counter or down counter, the carry or borrow signals are made high respectively.

DIGITAL CONTROLLED OSCILLATOR AND DIVIDER

DCO is the digital counterpart of the voltage controlled oscillator. Here control signals are used to modify the frequency of the DCO output.

There are two types of DCO usually used.

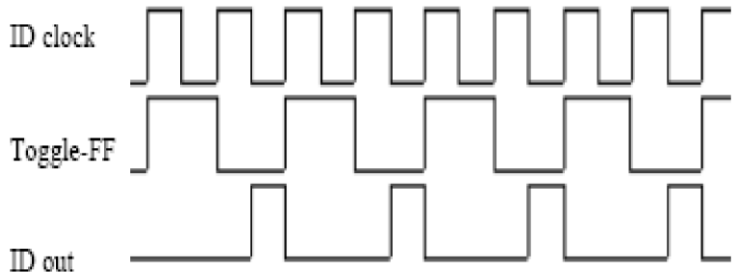
1. Divide by N counter type
2. Increment-Decrement counter type

A. Working

The carry and borrow are from the K-counter loop filter and the ID-counter is sensitive to positive edges. A Toggle-FF signal is generated following to the following rules:

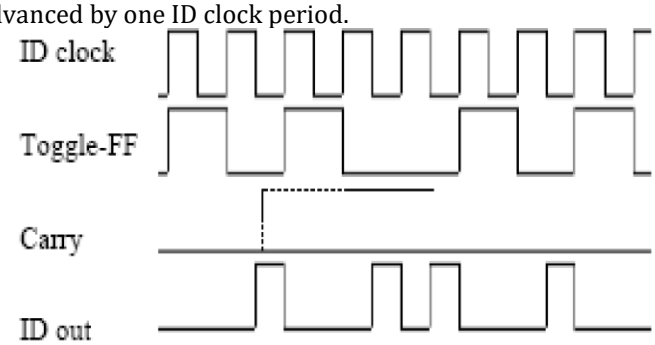
1. No BORROW or CARRY pulses

The toggle-FF switches on every positive edge of the ID clock if no CARRY or BORROW pulses are present.



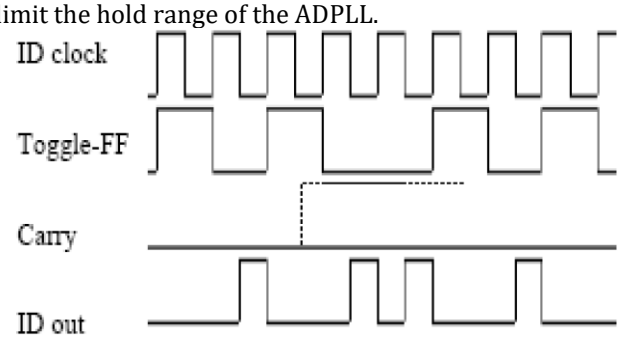
2. CARRY input applied when the toggle-FF is in the low state

When the toggle-FF goes high on the next positive edge of the ID clock but stays low for the next two clock intervals, the IDout is advanced by one ID clock period.



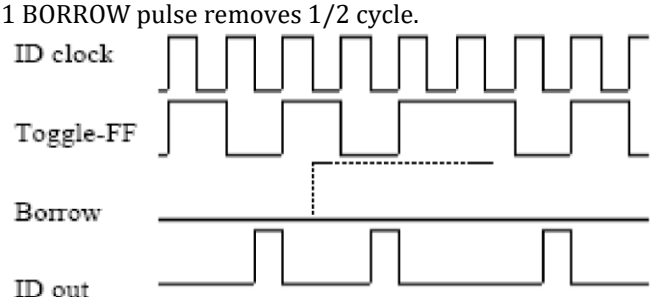
3. CARRY input applied when the toggle-FF is in the high state.

The toggle-FF is set to low for the next two clock intervals. Because the CARRY can only be processed when the toggle-FF is in the high state, the maximum frequency of the IDout signal is reached when the toggle-FF follows the pattern of "high-low-low-high-low-low". Therefore, the maximum IDout frequency = 2/3 ID clock frequency. This will limit the hold range of the ADPLL.



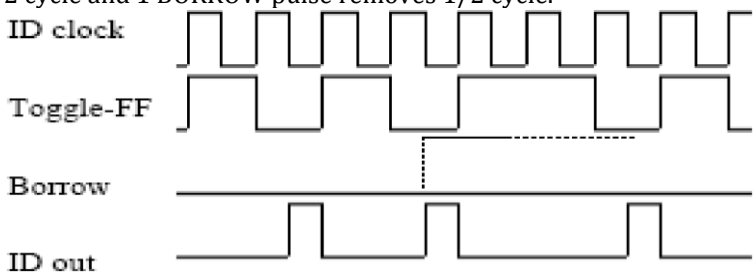
4. BORROW input applied when the toggle-FF is in the high

A BORROW pulse causes the toggle-FF to be set high on the succeeding two positive edges of the ID clock. This causes the next IDout pulse to be delayed by one ID clock period. The toggle-FF has the pattern of "low-high-high-low-high-high" which gives the min. IDout frequency = 1/3 ID clock frequency. Basically, 1 CARRY pulse adds 1/2 cycle and 1 BORROW pulse removes 1/2 cycle.

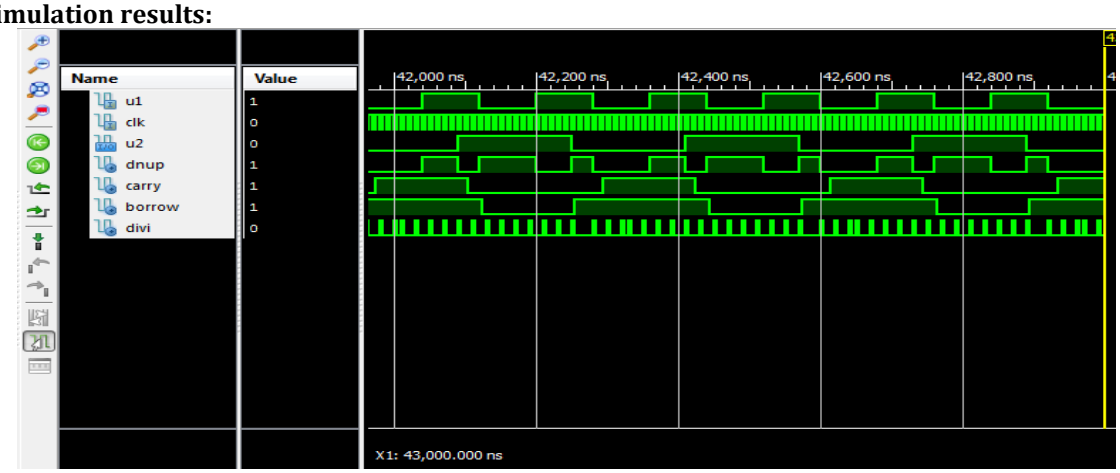


5. state BORROW input applied when the toggle-FF is in the low state

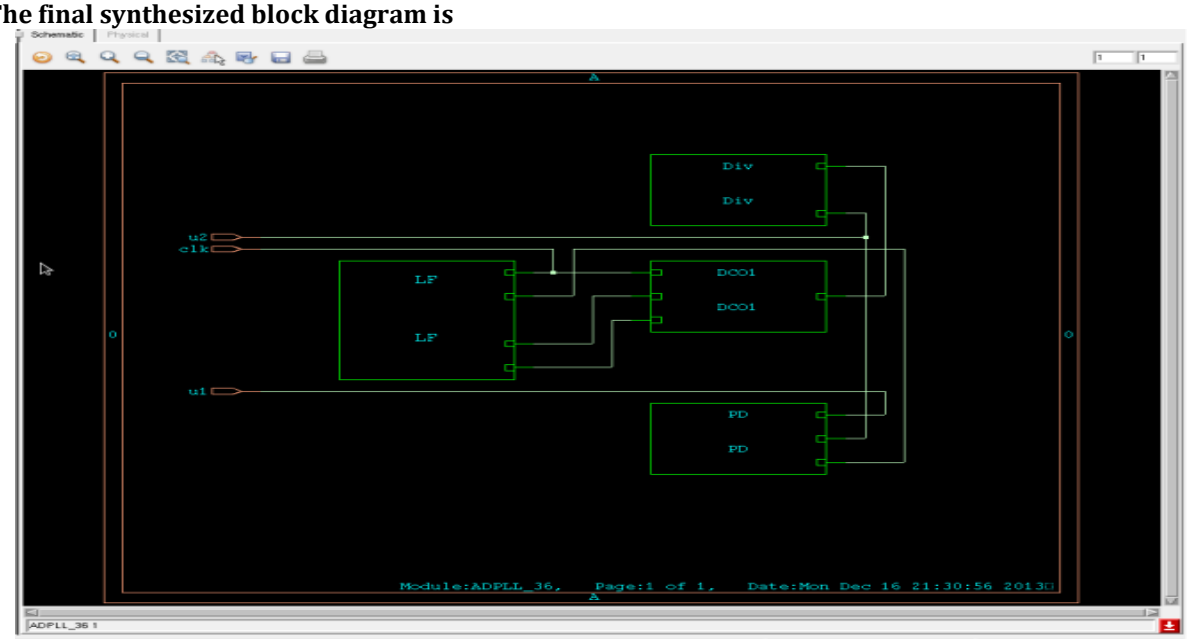
A BORROW pulse causes the toggle-FF to be set high on the succeeding two positive edges of the ID clock. This causes the next IDout pulse to be delayed by one ID clock period. The toggle-FF has the pattern of "high-high-low-high-low-high" which gives the min. IDout frequency = 1/3 ID clock frequency. Basically, 1 CARRY pulse adds 1/2 cycle and 1 BORROW pulse removes 1/2 cycle.



B. Simulation results:



The final synthesized block diagram is



CONCLUSION AND FUTURE WORK:

The Project discusses the implementation of ADPLL. Code for ADPLL is written in Verilog and compiled using NCVerilog. The proposed ADPLL consumes a power of 18.3 mW and an area of 376 μm^2.
The project was a really nice learning experience.
There are many Improvements and concepts that still need to be learned, but the basics of an all-digital PLL implementation was covered during this project. The design can be improved by implementing a full custom design. The extra clock input can be removed by implementing a clock independent Digital Control

Oscillator and replacing Loop Filter with a Time to Digital Converter (TDC). The PLL can be designed for a particular application such WiMax, GSM, etc

REFERNCES

1. V. Appleton, Automatic synchronization of triode oscillators, Proc. Cambridge Phil. Soc., 21(Part III):231 (1922-1923)
2. Henri de Bellescize, "La réceptionsynchrone," L'OndeÉlectrique (later: Revue de l'Electricité et de l'Electronique), vol. 11, pages 230-240 (June 1932)
3. B. Grebene, H. R. Camenzind, "Phase Locking As A New Approach For Tuned Integrated Circuits", in Proc. of ISSCC Digest of Technical Papers, pp. 100-101, Feb. 1969.
4. Roland E.Best, "Phase Locked Loops Design Simulation and Applications", McGraw-Hill, 5th Edition.
5. Shabaany, M.H., Saneei, M., "A 0.7-to-1.1-GHz all-digital phase-locked loop with a new phase frequency detector and controlled oscillator with body-biasing", in Proc. of 16th CSI International Symposium on Computer Architecture and Digital Systems (CADS), 2012, pp. 54 -59, May 2012
6. Kumm M., Klingbeil H., Zipf P, "An FPGA-Based Linear All-Digital Phase-Locked Loop", IEEE Transactions on Circuits and Systems I: Regular Papers, pp. 2487 – 2497 Vol.57 Issue: 9
7. A Das, S Dash, Sahoo A.K. , B C Babu, "Design and implementation of FPGA based linear all digital phase-locked loop", in Proc. of Annual IEEE India Conference (INDICON) 2012, pp. 280 – 285
8. S. Sharma, S. Vallabhaneni, S. Attri, N. Krishman, and R. C. Chauhan. "Design of an all-Digital PLL core on FPGA." http://klabs.org/mapld04/abstracts/sharma_a.doc
9. Saleh R. Al-Araji, M rihaZ. niassuH, dnaMahmoud A. Al-Qutayri "Digital Phase Lock Loops: Architectures and Applications", Springer, 1st edition
10. M Horowitz, C. Yang, S. Sidiropoulos. "High-speed electrical signaling: overview and limitations". in Proc. of IEEE Microelectronics conference 1999.
11. Bosco Leung, "VLSI for Wireless Communication", Springer, 2nd edition
12. KusumLatha and Manoj Kumar: ADPLL Design and Implementation on FPGA, 2013 International Conference on Intelligent Systems and Signal Processing (ISSP). P.no 272-277.