# NEW MULTILEVEL INVERTER TOPOLOGY FOR PHOTOVOLTAIC SYSTEM

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**ABSTRACT** This Paper proposes a single phase multilevel inverter configurations for renewable energy application especially photovoltaic system. The thirty-one level configuration of multilevel inverter reduces the value of total harmonic distortion. The half bridge inverter utilized in the thirteen level configuration increases the output voltage level to nearly twice the output voltage level of a conventional cascaded H-bridge multilevel inverter. The higher output voltage level is generated with lesser number of power semiconductor switches compared to thirteen level inverter configuration is illustrated by replacing the isolated DC sources in multilevel inverter with individual photo-voltaic panels using separate perturb and observe based maximum power point tracking and boost converters. The verification of the proposed system is demonstrated successfully using MATLAB/Simulink based simulation with constant irradiation and temperature conditions. Comparison is made between the thirteen level inverter configuration of 13.69%. The proposed thirty-one level inverter configuration with less a total harmonic distortion with less number of switches has a total harmonic distortion of 3.67%. Efficiency for thirteen level inverter is 95.80% and for thirty one level inverter is 98.31%.

**Keywords:** Photovoltaic, Cascaded H-bridge, multilevel inverter, boost converter, Maximum power point tracking, Integration of renewable source, Voltage source inverter.

## Introduction

Power electronic converters, especially dc/ac pulse width modulation(PWM) inverters have been extending their range of use in industry because they provide reduced energy consumption, better system efficiency, improved quality of product, good maintenance, and so on. In recent days, to address the concern postured by conventional energy sources, for example, exhaustion of fossil powers and atmosphere changes, numerous countries are expecting to build their share of energy generation from clean energy. Solar, wind, hydro and bio-fuel energies are the prime applicants of clean energy. Solar energy and wind energy have become more prominent when compared to the other renewable energy resources In India, Ministry of New and Renewable Energy (MNRE) has implemented to scale up the renewable target to about 175 GW by2022, with over 90% of this volume accounted by solar and wind-based power [1]. The installation of solar energy capacity has grown rapidly by 20-25% over the last few years in India because of numerous advantages offered such as reduced cost, pollution free and continuous availability in day time. The reason for decrease in solar cost is based on factors such as increasing the efficiency of solar cells, improvement of manufacturing technology and economies of scale. Maximum power point tracking (MPPT) plays a vital role in photovoltaic application for increasing the efficiency by tracking the maximum power from solar. Irradiation and temperatures are the two major factors which affect the generated voltage from photo voltaic (PV) system [2]. The usage of MPPT is to track the maximum power point during changes in the irradiation or temperature from the different approach for different problems therefore leading to high development times.

# **PWM TECHNIQUES**

The fundamental methods of pulse-width modulation (PWM) are divided into the traditional voltage-source and current-regulated methods. Voltage-source methods more easily lend themselves to digital signal processor (DSP) or programmable logic device (PLD) implementation [3]. However, current controls typically depend on event scheduling and are therefore analog implementations which can only be reliably operated up to a certain power level [4]. In discrete current-regulated methods the harmonic performance is not as good as that of voltage-source methods. A sample PWM method is described below.

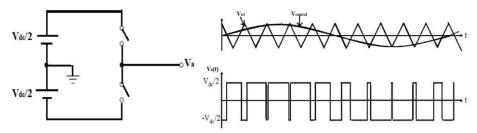


Fig.1 Pulse-Width Modulation technique

In the carrier-based implementation, at every instant of time the modulation signals are compared with the carrier and depending on which is greater, the switching pulses are generated [5]. In the PWM scheme there are two triangles, the upper triangle ranges from 1 to 0 and the lower triangle ranges from 0 to -1. In the similar way for an N -level inverter, the (N-1) triangles are used and each has a peak-to-peak value of 2/ (N-1). Hence the upper most triangle magnitude varies from 1 to (1-2/(N-1)), second carrier waveform from (1-4/(N-1)), and the bottom most triangle varies from (2-2/(N-1)) to -1.Carrier-based PWM scheme using the in phase disposition (IPD) can be seen in Figure below It is clear from the figure that during the positive cycle of the modulation signal, when the modulation is greater than Triangle 1 and Triangle 2, then S1ap and S2ap are turned on and also during the positive cycle S2ap is completely turned on.When S1ap and S2ap are turned on, the converter switches to the + Vdc / 2.When S1an and S2ap are on, the converter switches to zero and hence during the positive cycle S2ap is completely turned on and S1ap and S1an will be turning on and off and hence the converter switches from 0 to - Vdc / 2 [6]. The phase voltage equations for star-connected, balanced three-phase loads expressed in terms of the existence functions and input nodal voltage

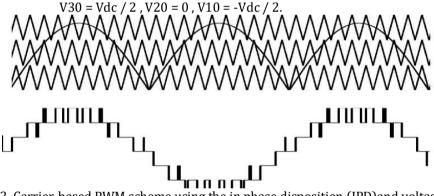


Fig:2. Carrier-based PWM scheme using the in phase disposition (IPD)and voltage output

# MAXIMUM POWER POINT TRACKING

Maximum power point tracking (MPPT) control is mandatory to generate maximum power from the PV panel and to obtain good performance when the climate changes (particularly irradiation and temperature) or the Standard Test Condition values deviates [4].By using this MPPT controller, the duty cycle is generated and is used for triggering the boost converter switch. The perturb and observer (P&O) algorithm for MPPT is the most popular algorithm due to its simplicity and ease of implementation in real time. After each perturbation, the P&O algorithm compares the value of power fed from the PV source before and after the perturbation. If the power has increased after the perturbation, the operating point moves towards the MPPT. After a voltage perturbation, the power drawn from PV decreases, the operating point has been moved away from MPPT hence the reverse perturbation direction is needed in the next perturbation cycle. The process is repeated continuously and the duty cycle is generated and fed to the boost converter. During the normal operation, the operating point continuously varies around the MPPT point. So, the PV system output voltage continuously oscillates, therefore, size of perturbation is important to maintain the MPPT condition as more perturbation size leads to more oscillation [5]. For this reason, perturbation voltage step size must be chosen carefully.

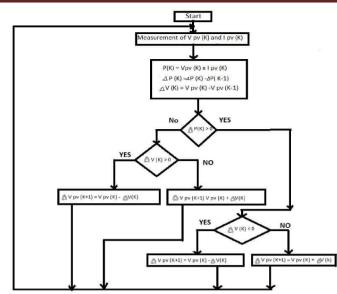


Fig 3. Perturb and Observer maximum power point tracking method.

## PV INTEGRATED SINGLE PHASE MULTILEVEL INVERTER

It consists of PV panels with Maximum power point tracking (MPPT), boost converter, multilevel inverter Cascaded H- Bridge Multilevel Inverter circuit. The CHBMLI circuit provides 13-level output voltage with the help of 14 switches and 4 sources whereas conventional CHBMLI requires 24 switches and 6 sources for generating the same output voltage level [6]. The separate DC source of multilevel inverter is replaced by separate PV panel with P&O MPPT and boost converter. Conventional CHBMLI requires 6 separate boost converters with same rating for generating the 13-level output voltage. But, the MLI requires only 4 separate boost converters for generating the same output voltage. Therefore, due to the reduction in the number of boost converters utilized, the cost of system comparatively reduces when compared to the conventional CHBMLI. Thus, the implemented system has the advantages such as reduced cost due to the elimination of transformers and small rating storage elements.

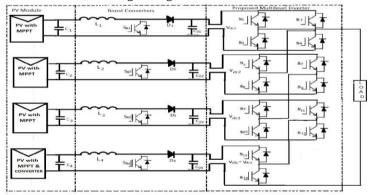


Fig 4. Single phase multilevel inverter integrated with photovoltaic panel.

| able :1  | . Switching sequer | ice of implemented MLI for 13-level output volt                                    |   |  |  |  |  |
|----------|--------------------|--|---|--|--|--|--|
| LevelsVo |                    | Combinations   | Switching combinations  |  |  |  |  |
|          | (output voltage)   |  |   |  |  |  |  |
| 1        | 0Vdc               | 0Vdc   | S1, S3, S5, S7, S9, S11,S14   |  |  |  |  |
| 2        | 0.5Vdc             | Vdcx   | S2, S4, S6, S8, S10, S12,S13  |  |  |  |  |
| 3        | Vdc                | Vdc1   | S1, S4, S6, S8, S10, S12,S14  |  |  |  |  |
| 4        | 1.5Vdc             | Vdc1+ Vdcx   | S1, S4, S6, S8, S10, S12,S13  |  |  |  |  |
| 5        | 2Vdc               | Vdc1+ Vdc2   | S1, S4, S5, S8, S10, S12,S14  |  |  |  |  |
| 6        | 2.5Vdc             | Vdc1+ Vdc2+ Vdcx   | S1, S4, S6, S8, S10, S12,S13  |  |  |  |  |
|          | Levels 1 2 3 4 5   | Levels Vo<br>(output voltage)<br>1 0Vdc<br>2 0.5Vdc<br>3 Vdc<br>4 1.5Vdc<br>5 2Vdc | Levels Vo<br>(output voltage)Combinations10Vdc0Vdc20.5VdcVdcx3VdcVdc141.5VdcVdc1+ Vdcx52VdcVdc1+ Vdc2 |  |  |  |  |

| Table :1. Switching sequence of implemented MLI for 13-level output voltage. |
|--|
|--|

| 7  | 3Vdc    | Vdc1+ Vdc2+ Vdc3  | S1, S4, S5, S8, S9, S12,S14  |
|----|---------|-------------------|------------------------------|
| 8  | -0.5Vdc | -Vdc1+ Vdcx       | S2, S4, S6, S7, S10, S12,S13 |
| 9  | -1Vdc   | -Vdc1             | S2, S4, S6, S7, S10, S12,S14 |
| 10 | -1.5Vdc | -Vdc1- Vdc2+ Vdcx | S2, S4, S6, S7, S9, S12,S13  |
| 11 | -2Vdc   | -Vdc1- Vdc2       | S2, S4, S6, S7, S9, S12,S14  |
| 12 | -2.5Vdc | -Vdc1- Vdc2- Vdc3 | S2, S4, S6, S7, S9, S11,S13  |
|    |         | +Vdcx             |                              |
| 13 | -3Vdc   | -Vdc1- Vdc2- Vdc3 | S2, S4, S6, S7, S9, S11,S14  |
|    |         |                   |                              |

The details of operating the switches and the combinations in 1ach level are shown in Table 1. The conduction of switches per voltage level is less when compared to conventional CHBMLI. So, the implemented MLI configuration generates higher number of voltage levels with less number of switches and conduction switches The mathematical expressions for generating the number of output voltage level areas follow:

 $L_v = 2 \times [(2 \times k) + 1] - 1$ .....(1) Where Lv= number of levels K=1,2,3,4,.....

## **Switching Scheme**

The switching scheme used is the Phase Disposition Pulse Width modulation (PDPWM). It uses both reference wave and carrier wave. Generally, 'Lv' level inverter requires 'Lv - 1'carriers to produce the required output voltage waveform. The amount of carriers is equally divided into two groups such as upper and lower carrier signals. The upper carriers are placed in above zero reference (positive side) while the lower carriers are placed in below zero reference (negative side). The sinusoidal reference is continuously compared with triangular carriers which generate the Boolean output. A simple logic operation is added with the Boolean output based on the switching table of the implemented MLI topology, which generates precise pulses for appropriate switches. This appropriate logic makes the output voltage waveform symmetrical.

(S1=C2), (S3=C4), (S5=C6), (S7=C7) (S8=C1), (S9=C9), (Sn=Cn)  $S2= (C1^*\sim C2) + (\sim C1^*C2) + C7$   $S4= (C1^*\sim C4) + (\sim C1^*C4) + C1(8)$   $S6= (C1^*\sim C6) + (\sim C1^*C6) + C1$   $S10= (C7^*\sim C9) + (\sim C7^*C9) + C7 S12= (C7^*\sim Cn) + (\sim C7^*Cn) + C1$   $S13=(C_1 \odot C2) + (C3 \odot C_4) + (C_5 \odot C_6) + (Cn \odot C!2)S14 = (C2 \odot C3) + (Q \odot C_5) + (C_8 \odot C_9) + (C_{10} \odot C11)$ Using C1 to C12 parameters and comparing Backage extract. The sympletic  $* \odot$  parameters

Here, C1 to C12 represents each carrier's Boolean output. The symbols+,  $\sim$ ,\*,©, represents logical OR, NOT, AND, and XOR respectively.

# LAYOUT OF THE THIRTY-ONE LEVEL INVERTER CONFIGURATION

This Topology consists of ten unidirectional power switches and four dc voltage sources. If the power switches of (*SL*,1, *SL*,2), (*SL*,3, *SL*,4), (*SR*,1, *SR*,2), and (*SR*,3, *SR*,4) turn on simultaneously, the dc voltage sources of *VL*,1, *VL*,2, *VR*,1, and *wVR*,2 will be short-circuited, respectively. Therefore, the simultaneous turnon of these switches should be avoided. In addition, *Sa* and *Sb* should not turn on simultaneously. The magnitudes of the dc voltage sources of the proposed 31-level inverter is recommended as follows: VL.1 = Vdc

VR,1 = 2Vdc VL,2 = 5Vdc VR,2 = 10Vdc

The proposed inverter generates all negative and positive voltage levels from 0 to 15 Vdc with steps of Vdc. It is important to note that the power switches in the mentioned topologies are unidirectional. In addition, other topologies based on bidirectional switches.

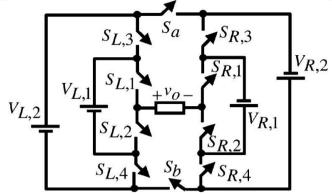


Fig 5.Layout of 31 level multilevel inverter

# Table 2 Represents switching sequence of 31 level multilevel inverter

|     |                     |              | <b>-</b>     |              | leening      | 5 Sequ        |               |              | -  |            |                          |
|-----|---------------------|--------------|--------------|--------------|--------------|---------------|---------------|--------------|----|------------|--------------------------|
|     | <i>a</i> . <i>i</i> | <i>a</i>     | <b>a</b> 0   | <i>.</i> .   | <b>a b c</b> | <b>6</b> 10 0 | <b>6</b> 00 0 | <b>a b</b>   | ~  | ~          |                          |
| NO. | SL,1                | <i>S</i> L,2 | <b>S</b> L,3 | <b>S</b> L,4 | <b>S</b> R,1 | <b>S</b> R,2  | <b>S</b> R,3  | <b>S</b> R,4 | Sa | <b>S</b> b |                          |
| 1 2 | 1<br>1              | 0            | 1            | 0            | 1            | 0             | 1<br>1        | 0            | 0  | 1          | VL,2+VR,2                |
|     |                     | -            |              | 0            | 0            |               |               | 0            | 0  | 1          | VL,2+VR,2-VL,1           |
| 3   | 0                   | 1            | 1            | 0            | 1            | 0             | 1             | 0            | 0  | 1          | VR,2+VL,2-VR,1           |
| 4   | 0                   | 1            | 1            | 0            | 0            | 1             | 1             | 0            | 0  | 1          | VL,2+VR,2-VL,1-VR,1      |
| 5   | 1                   | 0            | 1            | 0            | 1            | 0             | 0             | 1            | 0  | 1          | VL,1+VR,2                |
| 6   | 1                   | 0            | 1            | 0            | 0            | 1             | 0             | 1            | 0  | 1          | VR,2                     |
| 7   | 0                   | 1            | 1            | 0            | 1            | 0             | 0             | 1            | 0  | 1          | VL,1-VR,1+VR,2           |
| 8   | 0                   | 1            | 1            | 0            | 0            | 1             | 0             | 1            | 0  | 1          | VR,2-VR,1                |
| 9   | 1                   | 0            | 0            | 1            | 1            | 0             | 1             | 0            | 0  | 1          | VL,2+VR,1                |
| 10  | 1                   | 0            | 0            | 1            | 0            | 1             | 1             | 0            | 0  | 1          | VL,2+VR,1-VL,1           |
| 11  | 0                   | 1            | 0            | 1            | 1            | 0             | 1             | 0            | 0  | 1          | VL,2                     |
| 12  | 0                   | 1            | 0            | 1            | 0            | 1             | 1             | 0            | 0  | 1          | VL,2-VL,1                |
| 13  | 1                   | 0            | 0            | 1            | 1            | 0             | 0             | 1            | 0  | 1          | VL1+VR,1                 |
| 14  | 1                   | 0            | 0            | 1            | 0            | 1             | 0             | 1            | 0  | 1          | VR,1                     |
| 15  | 0                   | 1            | 0            | 1            | 1            | 0             | 0             | 1            | 0  | 1          | VL,1                     |
| 16  | 1                   | 0            | 1            | 0            | 1            | 0             | 1             | 0            | 1  | 0          |                          |
|     |                     |              |              |              |              |               |               |              |    |            | 0                        |
|     | 0                   | 1            | 0            | 1            | 0            | 1             | 0             | 1            | 0  | 1          |                          |
| 17  | 1                   | 0            | 1            | 0            | 0            | 1             | 1             | 0            | 1  | 0          | -VL,1                    |
| 18  | 0                   | 1            | 1            | 0            | 1            | 0             | 1             | 0            | 1  | 0          | -VR,1                    |
| 19  | 0                   | 1            | 1            | 0            | 0            | 1             | 1             | 0            | 1  | 0          | -(VL,1+VR,1)             |
| 20  | 1                   | 0            | 1            | 0            | 1            | 0             | 0             | 1            | 1  | 0          | -(VL,2-VL,1)             |
| 21  | 1                   | 0            | 1            | 0            | 0            | 1             | 0             | 1            | 1  | 0          | -VL,2                    |
| 22  | 0                   | 1            | 1            | 0            | 1            | 0             | 0             | 1            | 1  | 0          | -(VL,2+VR,1-VL,1)        |
| 23  | 0                   | 1            | 1            | 0            | 0            | 1             | 0             | 1            | 1  | 0          | -(VL,2+Vr,1)             |
| 24  | 1                   | 0            | 0            | 1            | 1            | 0             | 1             | 0            | 1  | 0          | -(VR,2-VR,1)             |
| 25  | 1                   | 0            | 0            | 1            | 0            | 1             | 1             | 0            | 1  | 0          | -(VL,2_VR,1-VL,1)        |
| 26  | 0                   | 1            | 0            | 1            | 1            | 0             | 1             | 0            | 1  | 0          | -VR,2                    |
| 27  | 0                   | 1            | 0            | 1            | 0            | 1             | 1             | 0            | 1  | 0          | -(VL,1+VR,2)             |
| 28  | 1                   | 0            | 0            | 1            | 1            | 0             | 0             | 1            | 1  | 0          | -(VL,2+Vr,2-VL,1-VR,1)   |
| 29  | 1                   | 0            | 0            | 1            | 0            | 1             | 0             | 1            | 1  | 0          | -(VR,2+VL,2-VrR1)        |
| 30  | 0                   | 1            | 0            | 1            | 1            | 0             | 0             | 1            | 1  | 0          | -(VL,2+VR,2-VL,1)        |
| 31  | 0                   | 1            | 0            | 1            | 0            | 1             | 0             | 1            | 1  | 0          | _(VL,2+VR,2)             |
| ~ - | 2                   | -            |              | -            | 2            | -             | -             | -            | -  | -          | _( · =,= · · · · · · - ) |

## SIMULATION RESULTS

The photovoltaic based boost converter along with P&O MPPT integrated with multilevel inverter is designed using MATLAB/SIMULINK.

The 13-level inverter voltage and current output is shown bellow

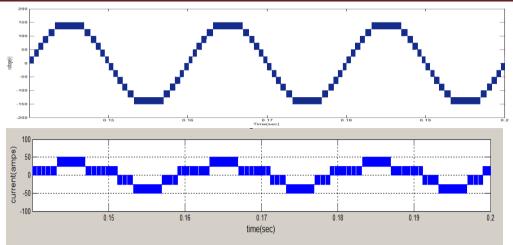


Fig 6. Output voltage and current waveform of 13- level inverter configuration

FFT analysis: The Total Harmonic Distortion (THD) level in the output is 13.87%

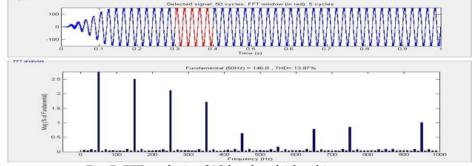
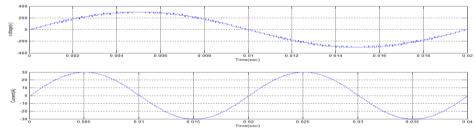
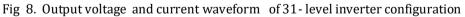


Fig 7. FFT analysis of 13 level multi-level inverter

# Simulation results for 31-level inverter configuration:

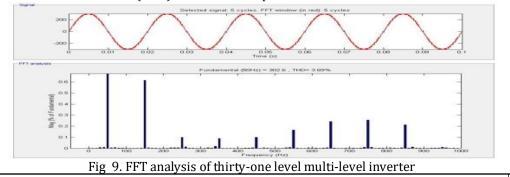
The 31-level inverter voltage and current output is shown below.





# FFT analysis:

The Total Harmonic Distortion (THD) level in the output is 3.69%



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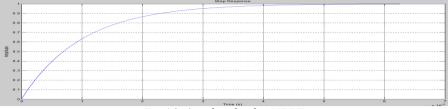
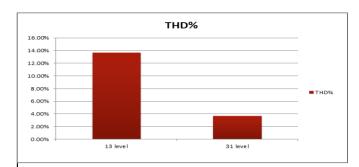
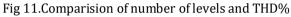


Fig 10. Amplitude for MPPT





Calculations

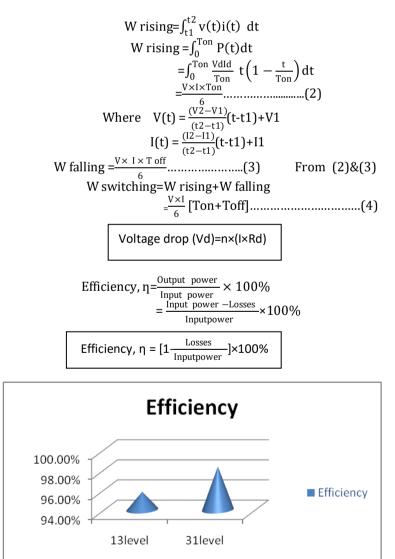


Fig:12. Efficiency of 13 and 31 level MLI

| Table: 3.Comparison between 13 level and 31 level I |   |                  |          |           |  |  |  |
|---|---|------------------|----------|-----------|--|--|--|
|   |   | Inverter         | Thirteen | Thirty-   |  |  |  |
|   |   | configuration    | level    | One level |  |  |  |
|   |   |                  |          |           |  |  |  |
|   | 1 | Switches         | 14       | 10        |  |  |  |
|   | 2 | Sources          | 4        | 4         |  |  |  |
|   | 3 | Voltage drop     | 6.5V     | 6.2V      |  |  |  |
|   | 4 | THD%             | 13.87%   | 3.69%     |  |  |  |
|   | 5 | Switching losses | 4.88W    | 3.54W     |  |  |  |
|   | 6 | Efficiency       | 95.80%   | 98.31%    |  |  |  |

#### I

## Conclusion

This paper presented single phase PV based multilevel inverter with thirteen levels and thirty-one levels. The verification of the proposed system is demonstrated successfully using MATLAB/Simulink based simulation with constant irradiation and temperature conditions. The thirteen level inverter configuration has a total harmonic distortion of 13.69%. The proposed thirty level inverter configuration with less number of switches has a total harmonic distortion of 3.67%. Efficiency for thirteen level inverter is 95.80% and for thirty one level inverter is 98.31%.

## Acknowledgement

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