A NOVEL LOW POWER AND NOISE TOLERANT TSPC FLIPFLOP DESIGN TECHNIQUE FOR BIOMEDICAL APPLICATION

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ABSTRACT: *CMOS based devices are highly recommended for low static power consumption and noise immunity. CMOS technology is used in various analog circuits like comparators, Amplifiers, Digital to Analog, Analog to Digital Converters, Phase Locked Loop(PLL) and many others. Here, in this paper we have studied various CMOS based PLL Circuits using different technologies like True Single phase Clock(TSPC), Injection Locked frequency Divider(ILFD) etc. to achieve low power consumption. A preset-able true single section clocked (TSPC) D flip-flop shows various glitches (noise) at the output thanks to unneeded toggling at the intermediate nodes. Preset- ready changed TSPC (MTSPC) D flip- flop have been projected as another resolution to alleviate this downside. However, the MTSPC D flip-flop needs one additional PMOS to suspend toggling of the intermediate nodes. during this work, we tend to designed a 2/3prescaler counter by modified D flip flop.*

Key Words: *D flip-flop, TSPC D flip-flop, modified TSPC D flip- flop.*

I. INTRODUCTION

One of the foremost vital classes of logic family that is needed for style any sorts of physical science system is consecutive logic circuits. D flip- flops (DFF) area unit the foremost vital basic building blocks of any digital terribly giant scale integrated circuits (VLSI).The performance of DFFs directly have an effect on the overall performance of the digital circuits. In order to get higher performances of the circuits, researchers have developed differing kinds of DFFs [5-11]. These structures may be divided into static and dynamic classes, but dynamic DFFs has higher performance in terms of power delay product (PDP). D flip- flops finds application in low power Phase locked loop (PLL) in numerous blocks of Multichannel PLL for tomograph [12]. Static D flip-flop is extremely slow once it should be employed in a megacycle frequency vary [1], therefore to avoid that, a TSPC D flip-flop in [13] is selected .but there area unit various glitches within the intermediate nodes, due to that the general performance of the circuit gets degraded.

In this paper we have a tendency to projected a changed positive edge triggered TSPC D flip-flop (MTSPC DFF) that is some extended version of positive edge triggered TSPC D flip-flop. The changed TSPC DFF suspends the Toggling of the intermediate glitches of nodes. As a result, the overall performance of the circuit is improved

EXISTING SYSTEM

The performance of DFFs directly affects the general performance of the digital circuits. so as to get higher performances of the circuits, researchers have developed differing kinds of DFFs. These structures may be divided into static and dynamic classes, but dynamic DFFs has higher performance in terms of power delay product (PDP). D flip-flops finds application in low power analog to digital device (ADC) in numerous blocks of Multichannel ADC for tomograph. Static D flip-flop is extremely slow once it's to be employed in a megacycle frequency vary, therefore to avoid that, a TSPC D flip-flop is chosen. but there area unit various glitches within the intermediate nodes, because of that the general performance of the circuit gets degraded.

II. PROPOSEDSYSTEM

In this section the prevailing positive edge triggered TSPC DFF and also the projected positive edge triggered MTSPC DFF area unit given. The projected MTSPC DFF isn't solely consumed low power however additionally it's the next most frequency of oscillation and PDP compared to TSPC DFF, as we are going to discuss shortly.

A. Operation of the existing TSPC DFF

In the existing positive edge triggered TSPC D Flip-Flop within the Fig. 1, once the clock signal Clk is LOW, the input is isolated from the output Qb, since the node B pre- charged to HIGH, and Qb maintains its older

price. onceClk is HIGH, node B won't be affected. thus once Clk is stable at either HIGH or LOW, the input is isolated from the output. onceClk makes a LOW-to- HIGH transition, the alphabetic characterb can latch the complement of the input and Q can pass the input to the output. once the predetermined input (RESET) is LOW the predetermined PMOS can get on and Qb maintains its price HIGH as long as RESET is LOW.

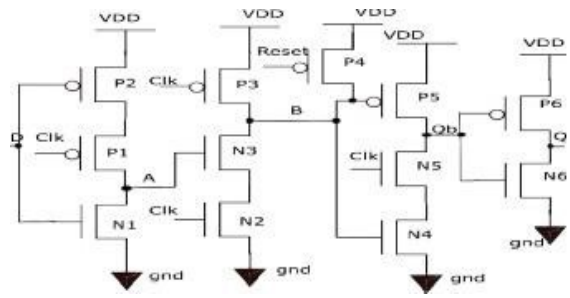

Fig 1: Positive edge triggered TSPC D Flip-flop

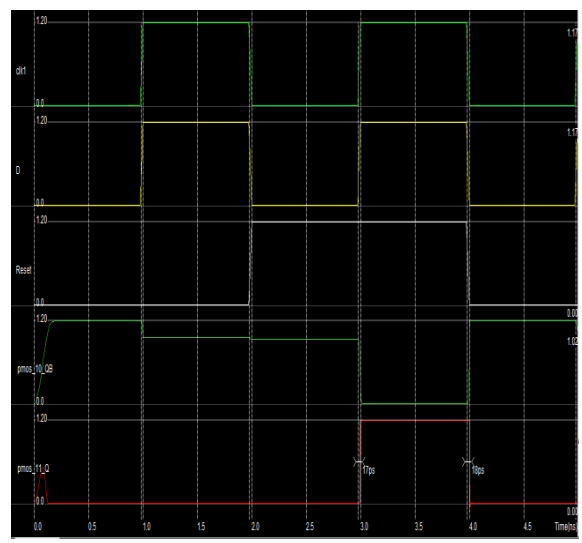

Fig 2: Simulation result of TSPC D Flip-flop

B. Operation of the proposed MTSPCDFF

Analysis of the behavior of node B reveals that for the times, once there is a path to ground, node B can continuously pre- charged to HIGH once clock (Clk) is LOW and can come back back to LOW once Clk is HIGH. So, whenever the input D is at a stable LOW for an extended time with relation to Clk, node B experiences continuous toggling. Such inessential behavior not solely accounts for big power consumption however is additionally a supply of noise on the output node, Q, caused by inaccurate glitches caused anytime Clk makes a LOW-to-HIGH transition. to resolve this downside, the projected MTSPC DFF design reveals that whenever the trail to ground is ON, pre- charging node B ought to be suspended to stop toggling. a straightforward technique that works here is to feature a PMOS semiconductor device that prevents the pre-charging section to occur while not moving the whole operation of the flip-flop.

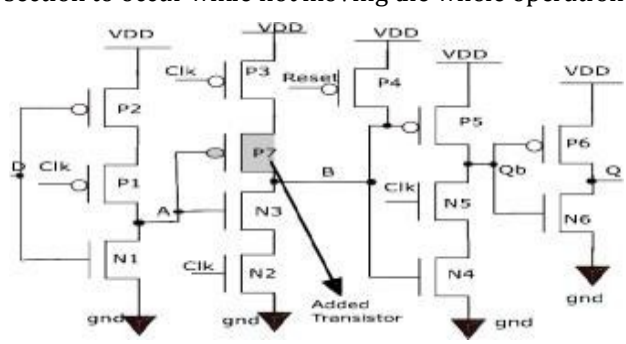

Fig 3: Positive edge triggered MTSPC D Flip-flop

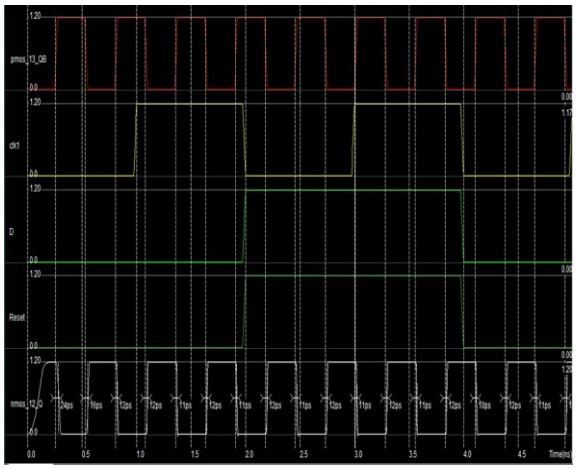

Fig 4: Simulation result of MTSPC D Flip-flop

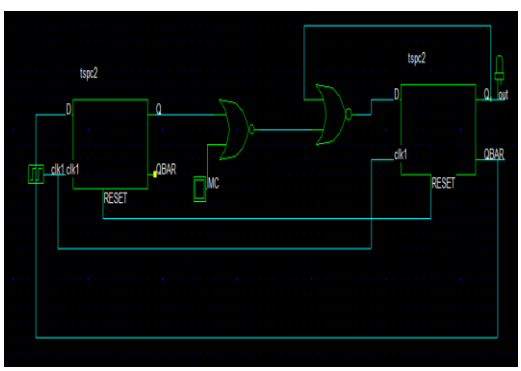

Fig 5: Prescaler diagram

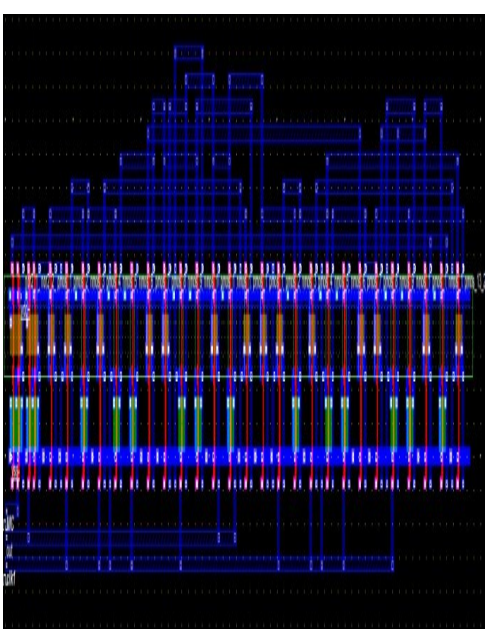

Fig 6: Prescaler layout

Performance Parameters	TSPC DFF	Modified TSPC DFF
Input clock frequency	1 GHz	1 GHz
Average Clock-to-Q delay	118.27 ps	91.99 ps
Setup time(tsetup)	70.13 ps	64.14 ps

Hold time(thold)	≈ 0	≈ 0
Average power consumption	465mW	411mW

Table 1: Comparison of existing and proposed system

III. CONCLUSION

In this work, a brand new preset-able changed true single section clocked (MTSPC) D flip-flop is projected. The technique utilizes a clocked dynamic logic. The projected methodology may be ran down to one gigahertz clock frequency, not like a TSPC D flip-flop based mostly preset-able 7-bit grey code counter which may be used up to five hundred megacycle clock frequency. The preset-able TSPC D flip-flop has a lot of noise at the output, this noise not solely have an effect on the output however additionally consumed terribly giant power. The projected preset-able MTSPC D flip-flop has terribly less noise at the output and consequently the power consumption is additionally terribly low. The projected preset-able MTSPC D flip-flop will be use quick, low power physical science world. By suspending the inessential toggling within the intermediate nodes of D flip-flop by adding one additional PMOS (as mentioned in MTSPC D FF).

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