DESIGN AND ANALYSIS OF DGS BASED PATCH ANTENNA WITH RECTIFIER FOR LOW POWER APPLICATIONS

Sathish M1, Amruth Balachandran2, Sriram Pasupathy2, Vignesh L2, Vignesh Karthi S2
1 Assistant Professor, 2UG Scholar
1,2 Department of Electronics and Communication Engineering, 1,2 Rajalakshmi Engineering College, Chennai-602105, India

Received: February 04, 2019 Accepted: March 23, 2019

ABSTRACT: This work’s objective is to design a Microstrip Patch Antenna (MSA) with high gain and better return loss. The basic MSA has been designed and different geometric variations have been performed on the basic MSA to obtain the desired radiation parameters. The MSA’s with the highest gain has been selected and optimized for the design frequency of 2.4GHz – 2.5GHz (ISM band). This is to be fabricated and tested. The received power is then passed through a rectification circuit and is translated from Alternating Current (AC) to Direct Current (DC), which is further used for low power applications.

Key Words: Microstrip Patch Antenna (MSA), Defected GroundStructure (DGS), Charge Pump, Wilkinson power divider.

I. Introduction

A patch antenna is a type of radio frequency antenna with a low profile, which can be mounted on a flat planar surface. It consists of a flat rectangular conducting sheet which can be used as a transmitter or receiver, (patch) mounted over a large rectangular conducting sheet called the ground plane. The ground and patch are made of Copper, coated with either Tin or Aluminium and are photo-etched on FR4 Epoxy ($\varepsilon_r = 4.4$) substrate. Slots and DGS are introduced onto the patch to improve the gain. Etched slots or defects on the ground plane of microstrip circuits are referred to as Defected Ground Structure (DGS). Single or multiple defects on the ground plane may be considered as DGS. The above has been integrated on the ground plane with the planar transmission line, that is, microstrip line, coplanar waveguide, and conductor-backed coplanar waveguide. The defects on the ground plane disturb the current distribution of the ground plane. The low pass filter is designed in order to eliminate the odd harmonics. The AC power sensed by the antenna is given to the rectifier circuit which produces DC voltage. Schottky diode SMS7630 having a low turn-onvoltage (240mv) and provides efficient rectification.

Section 2 of this paper investigates the design and optimisation of a patch antenna. Section 3 of this paper involves the analysis of DGS based patch antenna. In section 4, the concept of the antenna array is utilised to achieve a higher gain of the antenna of section 3. Finally, the rectifier circuit is designed and implemented to an array of DGS based patch antenna in section 5.
II. DESIGN AND ANALYSIS OF PATCH ANTENNA

The antenna proposed in this paper is designed on FR4 Epoxy substrate having a thickness of \( h = 1.6 \) mm. The dimensions are calculated using the formulas:

\[
W_p = \frac{1}{2f_r \sqrt{\varepsilon_{\text{eq}}}} \sqrt{\frac{2}{\varepsilon_{\text{eq}}+1} \frac{V_0}{2} \frac{2}{\varepsilon_{\text{eq}}+1}} \tag{1}
\]

where, \( V_0 \) is the speed of light in free space.

\( f_r \) is the resonant frequency of antenna.

\[
\varepsilon_{\text{eff}} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \sqrt{1+\frac{12}{\epsilon_r}} \tag{2}
\]

\[
\Delta L_p = \frac{0.412}{h} \left( \frac{\varepsilon_{\text{eff}}+0.3}{\varepsilon_{\text{eff}}+0.264} \right) \left( \frac{\varepsilon_{\text{eff}}-0.258}{\varepsilon_{\text{eff}}+0.8} \right) \tag{3}
\]

Where, \( \varepsilon_{\text{eff}} \) is effective dielectric constant.

\[
L_{\text{eff}} = L + 2 \Delta L_p \tag{4}
\]

\[
L_p = \frac{1}{2f_r \sqrt{\varepsilon_{\text{eff}}/\varepsilon_0}} - 2 \Delta L_p \tag{5}
\]

Using the formula's (1), (2), (3), (4) and (5) [13], the values are calculated and shown below in Table I and also the geometry of antenna is given below in Figure 2.

![Fig 2. The geometry of patch antenna](image)

### SPECIFICATIONS OF PATCH ANTENNA

#### TABLE I

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>DIMENSIONS (in mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( W_p )</td>
<td>36.05</td>
</tr>
<tr>
<td>( L_p )</td>
<td>29.40</td>
</tr>
<tr>
<td>( A )</td>
<td>7.6</td>
</tr>
<tr>
<td>( G )</td>
<td>0.3</td>
</tr>
<tr>
<td>( C )</td>
<td>9.75</td>
</tr>
<tr>
<td>( B )</td>
<td>14.33</td>
</tr>
<tr>
<td>( E )</td>
<td>51.22</td>
</tr>
<tr>
<td>( W_f )</td>
<td>2.133</td>
</tr>
</tbody>
</table>

III. DGS BASED PATCH ANTENNA

Slots and DGS are introduced onto the patch to improve the gain. The gain is increased due to the increase in current density along the non-radiating edge (\( l_p \)), which in turn increases the voltage along the radiating edge (\( w_p \)). This results in a denser electric field and better radiation pattern. Hence the gain is increased.
The introduction of DGS in the form of CSRR achieves the size reduction of the patch due to the sub-wavelength property of the CSRR. Studies have been performed on the various parameters affecting the patch due to the variation in slot and CSRR dimension and placements. The details for the same are provided. (Table II)

**Fig. 3.** The geometry of DGS based patch antenna.

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>DIMENSIONS (in mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rext</td>
<td>5.25</td>
</tr>
<tr>
<td>Rint</td>
<td>4.25</td>
</tr>
<tr>
<td>L_slot</td>
<td>4.00</td>
</tr>
<tr>
<td>W_slot</td>
<td>4.25</td>
</tr>
</tbody>
</table>

**TABLE II**

SPECIFICATIONS OF DGS BASED PATCH ANTENNA

**Fig. 4.** DGS based patch antenna (Ground view)

**Fig. 5.** Current distribution of DGS based patch antenna
IV. DGS BASED PATCH ARRAY

An antenna array is a series of multiple antennas connected together, that work together as one, to receive or transmit radio waves. Element spacing and the relative amplitude and phases determine the radiative property of the array. A feed is commonly used to connect multiple individual antennas. The antenna array has many advantages such as a high gain and wider bandwidth. Using the previously discussed patch with DGS and slot is implemented in an array format to obtain higher gain. A 1x2 array is implemented as shown in the next slide to increase the total gain by utilizing the compounded effect of the individual antennas. This array arrangement uses the Wilkinson power divider to distribute or combine the power from the two individual antennas equally, thus achieving better efficiency and making the impedance matching process relatively easier. The antenna array is implemented below (Figure 6) and the parameters are optimised using HFSS simulators and the results are shown in Figure 7.

![Fig. 6. The geometry of DGS based patch array using Wilkinson power divider](image)

The gain of DGS based patch antenna array is 6.8160 dB; the return loss is -33.4154 dB.

V. FILTER AND RECTIFIER DESIGN

The rectifier is a circuit that converts the RF signal into the DC signal. The diode used here is Schottky diode SMS 7630 due to the reasons cited previously (Section I). The low pass filter of order six is designed using ADS software (Figure 8). The Cockcroft–Walton (CW) voltage multiplier is an electric circuit that generates a...
high DC voltage from a low-voltage AC or pulsing DC input. During the negative half cycle of the sinusoidal input waveform, a diode (D1) is forward biased and conducts, charging the pump capacitor (C1) to the peak input voltage (Vp). As there is no return path for C1 to discharge into, it remains fully charged, acting as a storage device in series with the voltage supply. At the same time, diode D2 conducts via D1, charging up the capacitor, C2. In the positive half cycle, D1 is reverse biased, blocking the discharging of C1 while D2 is forward biased charging up C2. Since the voltage across capacitor C1 already equal to the peak input voltage, C2 charges to twice the peak voltage value of the input signal. In other words, V (positive peak) + V (negative peak), so on the negative half-cycle, D1 charges C1 to Vp and on the positive half-cycle, D2 adds the AC peak voltage to Vp on C1 and transfers it all to C2. The voltage across C2 discharges through the load, ready for the next half cycle. Then the voltage across C2 can be calculated as: Vout = 2Vp (subtracting the voltage drops across the diodes used) where Vp is the peak value of the input voltage. Note that this double output voltage is not instantaneous but increases slowly over each input cycle, eventually settling at 2Vp. As C2 only charges up during one-half cycle of the input waveform, the resulting output voltage discharged into the load has a ripple frequency equal to the supply frequency, hence the name half-wave voltage doubler. The disadvantage of this is that it can be difficult to smooth out this large ripple frequency, much similar to the half-wave rectifier circuit. Also, C2 must have a DC voltage rating of at least twice the value of the peak input voltage. The circuit for six stages CW charge pump is given below (Figure 9).

Fig. 8. Butterworth low pass filter of order six

Fig. 9. Rectifier circuit (CW voltage multiplier)

Fig. 10. Rectifier output
VI. CONCLUSION
The antenna array was designed for 2.45 GHz with HFSS and a gain of 6.8 dB is obtained. A butterworth low pass filter of order six was designed to eliminate odd harmonics and a six stage Cockcroft–Walton(CW) charge pump is used to rectify and boost the received voltage to 0.9 volts.

REFERENCES
2. DGS based microstrip patch antennas for UWB systems; Rakesh Kumar Yadav; Sushrut Das; R. L. Yadava.
3. Multiband DGS based microstrip patch antenna for open satellite communication; Amit Singh Bhadouria; Mithilesh Kumar.
10. PRINCE MAHDI MASUD; “A methodology for designing 2.45 GHz wireless rectenna system utilizing Dickson Charge Pump with Optimized Power Efficiency.” A thesis presented to the University of Waterloo in fulfillment of the thesis requirement for the degree of Master of Applied Science in Electrical and Computer Engineering.