SYNTHESIS OF REVERSIBLE LOGIC CIRCUITS

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ABSTRACT: : *With the advancement in VLSI technology, more and more devices can be now integrated on a single unit area which is helping in making more portable devices which uses less power. With the decrease in the size of the device, power dissipation is becoming major concern for the designing .For building low power circuits, the technologies like DNA Computing, quantum cellular automata, quantum computing, nano technologies, to remodel logics which can conserve energy and thus dissipates no power .the replacement of reversible logic application in quantum computation, there is a requirement of piling reversible computational and sequential circuits. The reversible logic is completely specified by n-input-output Boolean function that is each input assignment to an individual output and vice versa. In future technologies, reversible logics have great importance. This paper launches an access to synthesize reducing the garbage bit and gates which are used to make circuits, which is the chief dispute of reversible logic synthesis. In the suggested full-adder circuit reversible logic gates used are three as unlike earlier where four gates are required to make full adder . Thus,number of gates used is less in proposed circuit.*

Key Words: *Reversible Logic Gates, Garbage Output, QuantumCost, PrimitiveGates, Power Dissipation.*

I. INTRODUCTION:

With the advancement in technology, more and more portable devices are constructed by integrating more number of devices, thus because of the reduction in the size, power dissipation is becoming a major issue. In 1960, According to R. Landauer, irreversible circuits dissipated more energy due to the loss in information. Landauers principle states that, one bit of informationif lost, total energy equals to KT*ln (2) joules Energy will be dissipated,Boltzmann's constant 'k' and is equal to $1.38x10^{-23}$ J/K, and absolute constant is 'T' in Kelvin [1]. According to Landauer and Bennett, for no dissipation of any heat, all the operation in computation should be performed in reversible order. The first condition is if the input and output are uniquely revertible that is if input and be revertible from output then the circuit is logically reversible. The second condition is if the operation on the device can be performed in backward order then device is physically reversible no heat dissipates then. According to Thermodynamics' second law if the system is in thermodynamic equilibrium or is undergoing reversible process then total entropy of the system remains constant. Thus, in irreversible circuits if the data is lost once, the recovery is not possible which will lead to the loss of energy also. In 1973, Bennett stated that to reduce power dissipation, the information should not be lost and for that the circuits should be made by using reversible logic circuits [7]. Moore's law stated that in every 18 months, number of transistors doubles. The information does not mislay in Reversible circuits [8]. In quantum computing, reversible logics are used [3]. For Reversible computation only, reversible gates are used in which the output vector can be used to regain input vector, and this is possible because of unique one-to-one mapping in reversible gates. [4-5].

II. DEFINITIONS RELATED TO REVERSIBLE LOGIC:

a) Constant inputs:

It is broached that as to synthesize the logical function, the input mustbe either 1 or 0[8].

b) Reversible logic gate:

In Reversible circuits the operation can be conducted in reversible order, which allow the production of inputs from outputs and consumes zero power, in these reversible circuits, reversible gates are used for realization of Boolean functions.[3].

c) Garbage outputs:

Number of input should be equal to the number of outputs to maintain the reversibility of the circuit. Thus, the sum of number of inputs with constant input should be equal to addition of number of outputs with garbage output. [6]

d) Quantum cost: Cost of primitive gates is used to define the cost of circuit which is called the quantum cost of that circuit quantum cost can be calculated by number of primitive logics used to realize the circuit, should be known.[10].

III. BASIC REVERSIBLE GATES:

3.1Feynman gate

Feynman gate is proposed using two Billiard Ball Model gates. Input in Feynman gates are (m,n) which are mapped with output (q,r).[2]

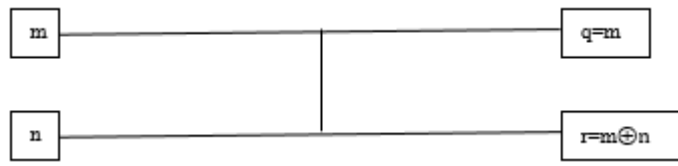

Figure3.1 (a)

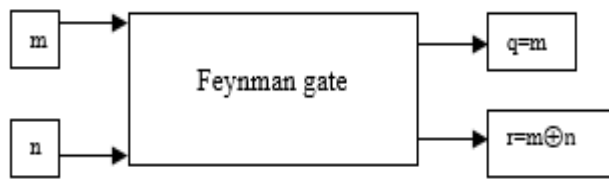

Figure3.1 (b)

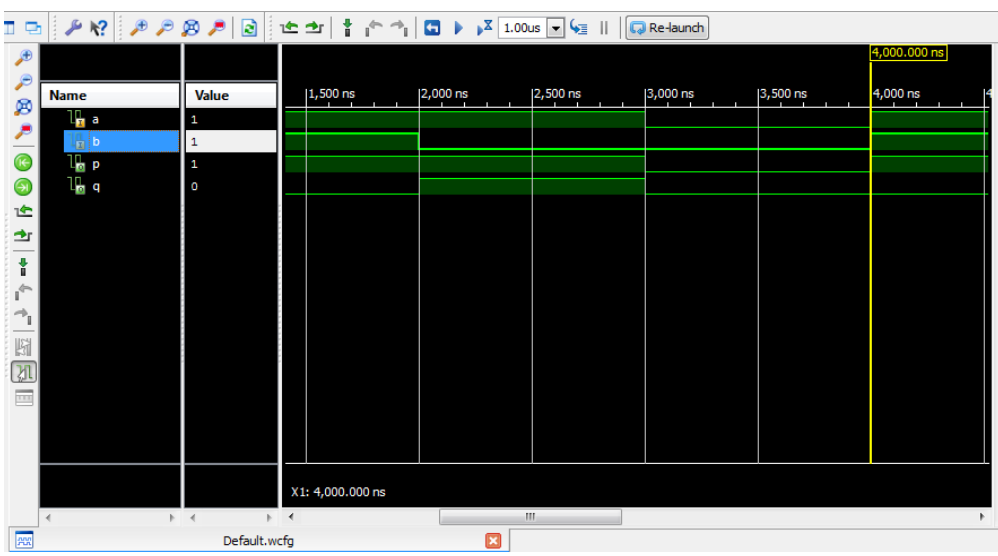

Figure3.1(c)

Figure3.1 (a) Quantum implementation, (b)Feynman gate, (c)Simulation of Feynman gate

It is a reversible gate with three inputs and outputs. The number of primitive gates used in Feynman gate is 1.The inputs (a, b, c) associates with outputs (p, q, r) Quantum cost is 1.

3.2 Peres gate

Itis a reversible gate which consists of two XOR gates and one AND gate and four primitive gates are used in Peres gate.The reversible 3*3 gate mapped input (m,n, o) withoutput (q, r, s). Quantum cost of Peres gate is four.[6]

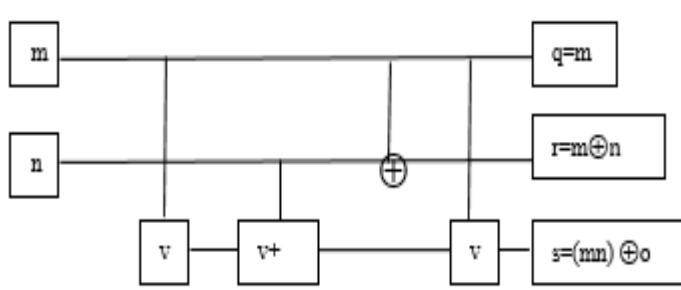

Figure3. 2 (a)

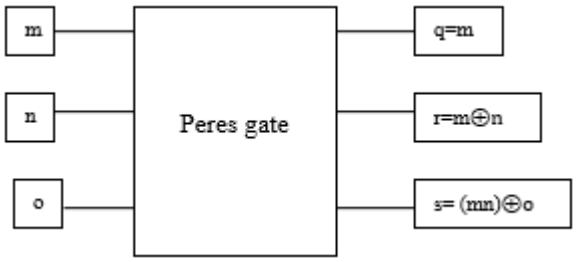

Figure3.2 (b)

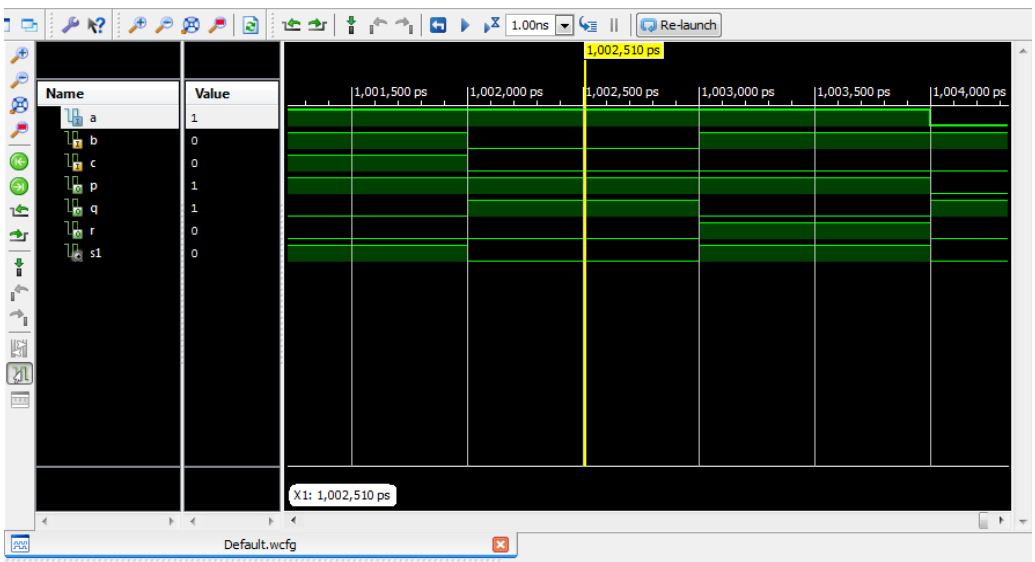

Figure3. 2(c)

Figure 3.2(a) quantumimplementation, (b)Peres gate, (c)Simulation of Peres gate

Peres gate has three inputs (a, b, c)mapped with outputs (p, q ,r). Number of primitive gates used for realization of peres gate are 4.[7]

3.3TOFFOLI GATE

Tommaso Toffoli invented toffoli reversible. It is also called as universal reversible logic gate this means toffoli gate can be used for construction of any other gate. It hasthree-bit input and outputs, total number of primitive gates used in Tofolli gate is four. The reversible 3*3 gate with quantum cost four having input (m,n,o) mapped with output (q, r,s).[10]

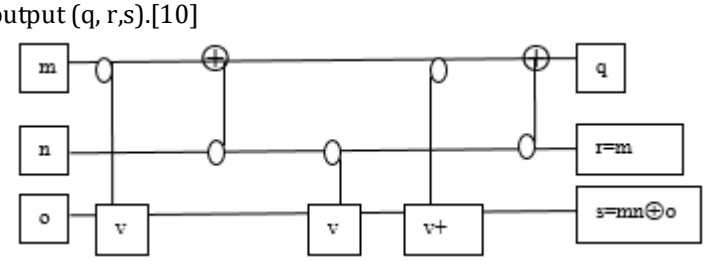

Figure 3.3 (a)

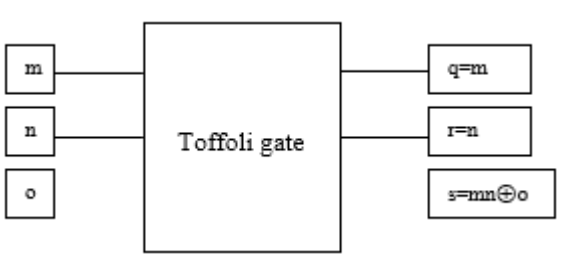

Figure3. 3(b)

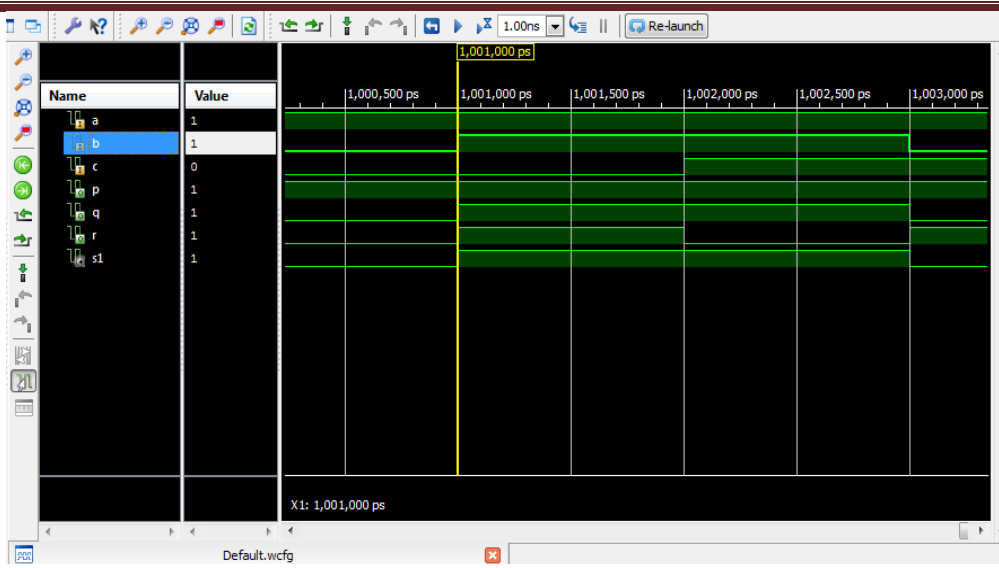

Figure3.3 (c)

Figure3.3(a)quantum implementation, (b)Tofolli gate(c) Simulation of Toffoli gate

As any reversible gate can be constructed using toffoli gate thus this gate is also called as universal gate. Five primitive gates are used to realize toffoli gate.

3.4Fredkin gate

Fredkin gate is invented by Edward Fredkin and is suitable for reversible computing which is a computational circuit having three input and output that sends first bit as it is; that is unchanged and if the first bit is '1' then it swaps the last two bits. Total number of primitive gates used in Fredkin gate is 5. In fredkin gate input (m, n, o) is mapped with output (q, r, s).[5]

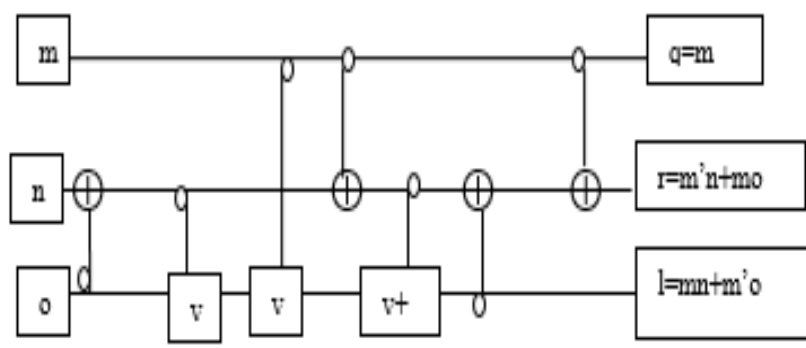

Figure 3.4(a)

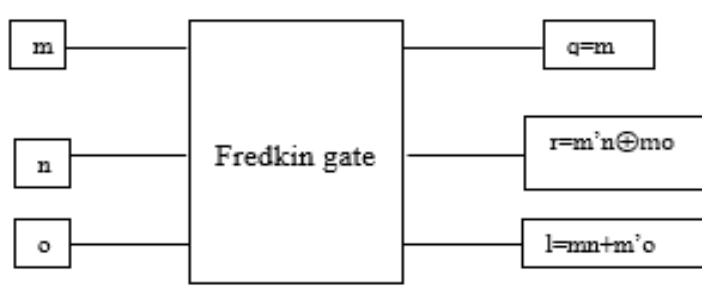

Figure 3.4(b)

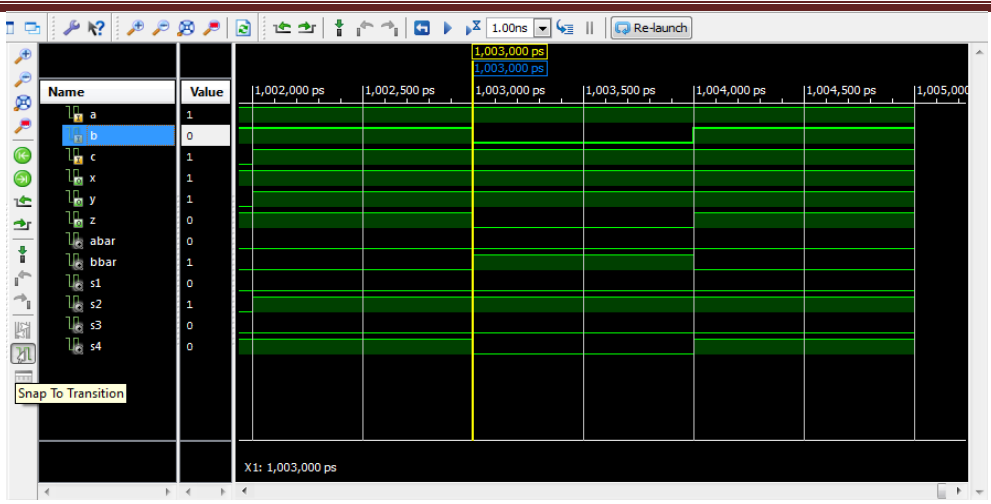

Figure3. 4(c)

Figure3. 4(a) quantumimplementations, (b)Fredkin gate, (c) Simulation of Fredkin gate

Edward Fredkin invented Fredkingate. For reversible computing, Fredkin gate is suitable as it is a computational circuit. The Fredkin gate has three inputs-outputs thattrade last two bits only if the first bit is 1 and transmits the first bit unchanged.

IV.PROPOSED PERES FULL ADDER:

For building reversible combinational and sequential circuits, peres gate is widely used. Peres gate is 3 × 3 gate that is it has three inputs which is uniquely mapped with three outputs.

Inputs of Peres Gate are represented as A, B, Cin and the outputs are referred as G1, G2, S, Cout.For construction of reversible full adder two peres gates are used. The connections required are as follows. The input Cin is grounded There are two garbage outputs here which are G1 and G2.

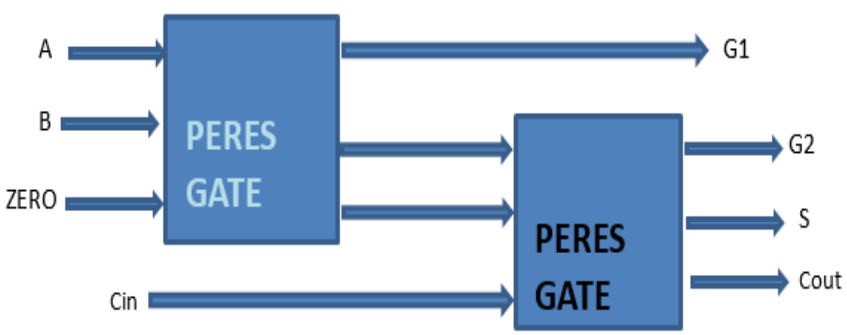

Figure 4(a) Peres gates used for Full Adder

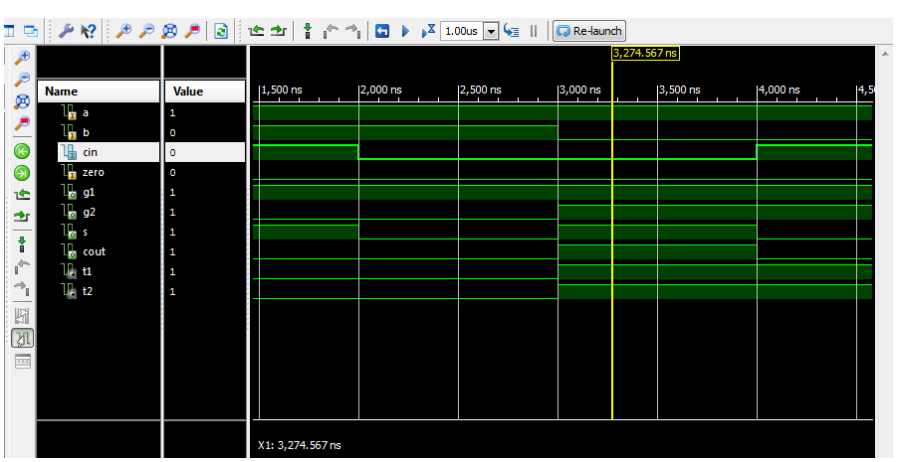

Figure4 (b)

Figure4 (a)Full Adder using Peres gate, (b) Simulation of reversible full adder

Three input combinations (011,101,110) we are getting the same output, hence to ensure unique input to output mapping we require two additional outputs (known as garbage outputs i.e. unutilized outputs). Also, the number of input and output bits is required to be same hence an extra input is added. The value for this extra bit can be set either0 or 1 depending upon the ease of the implementation of function of primary outputs i.e. S and C. Therefore, a reversible full adderhas four inputs and output given as (A, B, Cin, zero) and (G1, G2, S, Cout) respectively.

V.COMPARISON TABLE

COMPOSITION OF FULL ADDER	NUMBER OF GATES USED	GARBAGE OUTPUT	QUANTUM COST
PROPOSED PERES GATE	2	2	8
FEYNMAN GATE	3	3	-
TOFOLLI AND FEYNMAN GATE	4	2	-
FREDKIN GATE	4	3	20

Table 5.1 Comparison of Composition of Full Adder using different Reversible gates.

By the above comparison it is proved that Peres gates are more efficient for making of Full Adder as compare to any other reversible gates as no of gates used and garbage output is very less .

CONCLUSION:

This paper proposes design of conventional basic, universal gates and combinational circuits like full adders using reversible logic. The main aim is to realize these with minimum quantum cost, garbage outputs and delay and this is required so that optimization of any complex digital application can be attained. The Proposed circuits using reversible gates are verified using Xilinx14.2 tool by developing VHDL code. Reversible logic gates are used to build Combinational circuits as to reduce the number of gates resulting in reduction of delay and power dissipation has also reduced.

REFERENCE:

1. L.Benini ,A.Bogliolo and De micheli " a survey of desigm techneques for system –level dynamic power management:" IEEE transactions on VLSI ,pp.299-316,June 2000.
2. Pablo Aguirre and Fernando Silveria "Optimizing analog IC design when every nano amp counts",July 17,2012.
3. N.Ranganathan "Design of reversible sequential –cuits optimizing quantum."
4. R.Landaure "Irreversibility and heat generation in the computation process". IBM Journal of research and Development 5,pp.183-191,1961.
5. H.Lekatas and W.Wolf "Code Comparison for Low Power Embedded System".DAC-37.,Los Angeles ,California ,June 2000.
6. D.Mas and G.W Dueck "Reversible cascade with Minimal garbage" pp.1497-1509,November 2004.
7. Mike Frank "Quantum Computer Architecture for Physical Simulation" May 2000.
8. Yang G,Song X,Hung WNH and Marek Perkowski, "Bi-Direction Synthesis for Reversible circuit" IEEE computer society ,VLSI design 2007.
9. Vlatko vedral,Adriano bareno and artur ekert "quantum network for elementary arthematic ,nov 1995.
10. Thapilya and N rAnganathan ":design of reversible optimizing quantumin ISSN 2151-9617.
11. Frank "bi-direction computer architecture for physical simulation" for physics modeling workshop May 2000.

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